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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,118	11/18/2003	Katsumi Shibayama	46884-5179 (210649)	2756

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

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09/02/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,118	SHIBAYAMA ET AL.	
	Examiner	Art Unit	
	STEVEN H. RAO	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-28* is/are pending in the application.

4a) Of the above claim(s) *17-256* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,3-16, 26-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

A pre Appeal Breif review Conference was held on June 06, 2009 wherein it was decided to withdraw the Office Action mailed on 12/02/2008 and mail the following action.

Therefore Claims 1, 3-16 and 26-28 as recited in the amendment of 08/29/08 are currently pending in the Application.

Information Disclosure Statement

No further Ids after the one filed Jan, 09, 2008 has been filed in this case.

Election/Restrictions

Applicants' failure to fully reply to the request for complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.
Applicants' failure to reply constitutes any filings there after improper , but to move the case forward further action is taken any further incomplete replies will result in non entry of further fillings.

Claim Rejections - 35 USC Section 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,3-15 and 26-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Bauer etal. I(U.S. Patent .no. 2002/0011640, herein after Bauer).

With respect to claim 1 Bauer describes a back illuminated photodiode array comprising ; a first conductive type semiconductor substrate having a light-incident surface (figure 2 # 2 para 0013 line 2).

An opposite surface with a plurality of recessed portions located opposite said light-incident surface (Bauer fig.2)

The remaining limitations of claim 1 are :

a plurality of spatially separated second conductive type semiconductor regions wherein one of said second conductive type regions is located at each bottom of said recessed portions; (Bauer fig.2 # 4) wherein said second conductivity type semiconductor regions each individually constitute pn junction together with said first conductive type semiconductor substrate. (Fig. 2 # 5 para 0013). wherein said first conductive type semiconductor substrate is thinner in said recessed portions of said first conductive type substrate than in portions of said first conductive type semiconductor substrate located around said recessed portions. (Bauer fig.2, paras 0016 and 0019).

With respect to claim 3 Bauer describes a back illuminated photodiode array

according to claim 1, wherein said first conductive type semiconductor substrate is composed of a single semiconductor substrate. (Bauer fig.2 32, para 0012)

With respect to claim 4 to the extent entered Bauer describes a back illuminated photodiode array according to claim 1, wherein said first conductive type semiconductor substrate comprises a first semiconductor substrate including said light- incident surface and a second semiconductor substrate bonded to said first semiconductor substrate and including side walls of said recessed portions. (Bauer fig.2 # 2, bottom –light incident, top bonded to layers 3-4)

With respect to claim 5 Bauer describes a back illuminated photodiode array according to claim 4, further comprising an etching stop layer existing between said first semiconductor substrate and said second semiconductor substrate and having resistance to a specific etching agent to be used for said second semiconductor substrate. (Bauer , fig.2, first etch leaving areas of 6 and second etch leaving areas of 3 etc. it is inherent for a stop layer to be resistant to the etching agent for substrate in order for the stop layer to function as a stop layer).

.

With respect to claim 6 Bauer describes a back illuminated photodiode array according to claim 4, further comprising an insulation layer existing between said first semiconductor substrate and said second semiconductor substrate. (Bauer

para 0002 barrier layer, buffer layer, etc.)
).

With respect to claim 7 Bauer describes a back illuminated photodiode array according to claim 1, comprising a plurality of electrode pads each formed on a top surface of each said frame pad and individually and electrically connected to each said second conductive type semiconductor region, respectively (Bauer fig.2 # 8.1,8.2 etc) .

With respect to claim 8 Bauer describes a back illuminated photodiode array according to claim 7, further comprising: an electric insulation layer formed on each said frame pad; (Bauer para 0002; also well known in art e.g see-Chappo col. 7 lines 23-31, Mattson co1.5 lines 24-25) and a conductive member formed on said electric insulation layer and electrically connecting said second conductive type semiconductor regions with said electrode pads. (Bauer figure 2 , para 0017).

With respect to claim 9 Buaer describes a back illuminated photodiode array according to claim 8, wherein said electric insulation layer is provided with a contact hole for connecting an end of said conductive member to said second conductive type semiconductor regions. (Buaer fig.e well known see-also Chappo figure 10).

With respect to claim 10 Mattson describes a back illuminated photodiode array according to claim 1, where In each said second conductive type semiconductor region extends from the bottom of the respective recessed portion at which it is located to side surfaces of said respective recessed portion. (Chappo figure 10, col. 1 lines5-7).

With respect to claim 11 Bauetr describes a back illuminated photodiode array according to claim 1: wherein each said second conductive type semiconductor regions extend from the bottom of the respective recessed portion at which it is located over side surfaces of said respective recessed portion to a top surface of the respective frame pad framing said respective recessed portion. (Bauer fig. 2).

With respect to claim 12 Bauer describes a back illuminated photodiode array according to claim 11, comprising: an electric insulation layer formed on each said frame part and having a contact hole opposing the top surface of each said frame part ; and electrode pads electrically connected to said second conductivity type semiconductor regions through each said contact hole. (rejected for reasons under claims 5-9 , etc. above).

With respect to claim 13 Bauer describes a back illuminated photodiode array according to claim 1, wherein each said frame part comprises a first conductive type separation region having higher impurity concentration than said first conductive type semiconductor substrate.(well known e.g see Chappo col. 12

line 47-49, as Chappo's semiconductor substrate described in col. 6 lines 6-8 is not doped and first conductive type separation region on frame is doped, the first conductive type separation region has higher impurity concentration than the substrate).

With respect to claim 14 Buaer describes a back illuminated photodiode array according to claim I wherein an opening' size of said recessed portions decreases with an increase in the depth of said recessed portions Bauer fig.2 also well known in the art to decrease recessed portion, see Mattson figures).

With respect to claim 15 Bauer describes a back illuminated photodiode array according to claim 1 , wherein said light-incident surface side of said first conductive type semiconductor substrate is provided with a first conductive type accumulation layer having a higher impurity concentration than said first conductive semiconductor substrate. (Buaer para 0014 different band gaps formed by different concentrations also Chappo col. 12 line 47-49, as Chappo's semiconductor substrate described in col. 6 lines 6-8 is not doped and first conductive type separation region on frame is doped, the first conductive type separation region has higher impurity concentration than the substrate and fig. 14 ,vias and conductive type accumulation layer on first surface and col .12 lines22-25).

With respect to Claim 27 Bauer describes a back illuminated photodiode array according to claim 1, wherein each said frame part has a top surface covered by a film on which a wiring layer is present, and a passivation film is present on at least a portion of the wiring layer that covers a portion of the film on the top surface of the frame part, such that the film, wiring layer and passivation film extend along a side of the frame part into the recess framed by the frame part. (Bauer fig. 2).

With respect to Claim 26 Bauer describes a back-illuminated photodiode array (fig.2) comprising a semiconductor substrate, wherein only one side of said semiconductor substrate has a plurality of recesses (figure 2), and wherein each shape of openings of said recesses is square.(Buaer fig.2 see also well knon in theart Chappo figs. 2b and 17 similar to Applicants' figure 1, see also col .6 line 39-46, col. 13 line 29-41, col .2 line 49-54 square sub module 22 fits in recess of similar shape).

With respect to Claim 28 Bauer describes a back-illuminated photodiode array according to claim 26, further comprising a plurality of frame parts, each framing one of said recesses, wherein each said frame part has a top surface covered by a film on which a wiring layer is present, and a passivation film is present on at least a portion of the wiring layer that covers a portion of the film on the top surface of the frame part, such that the film, wiring layer and passivation film extend along a side of the frame part into the recess framed by the frame part. (Buaer fig. 2)..

B. Claim 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Bauer (U.S. Patent Publication No. 2002/0011640, herein after Bauer) as applied to claims 1-15 above and further in view of Yamanaka et al. (U.S Patent No. 6,372,558, herein after Yamanaka).

With respect to claim 16 Bauer describes a back illuminated photodiode array according to claim 4, wherein mutually opposing surfaces of said first semiconductor substrate and said second semiconductor substrate are different in their crystal plane orientation.

Bauer describe a back illuminated photodiode array according to claim 4 but do not specifically describe the first and the second semiconductor substrates to be different in their crystal plane orientation.

However, Yamanaka in figure 8A and col. 13 line 60- col. 14 line 20 describes the first and the second semiconductor substrates to be in different in their crystal plane orientation to increase stability of the device increase productivity and enhance mechanical and electronic properties of the surface.

Therefore it would have been obvious to one of ordinary skill in the art at the

time of the invention to include Yamanaka's the first and the second semiconductor substrates to be in different in their crystal plane orientation In Bauer's device to increase stability of the device increase productivity and enhance mechanical and electronic properties of the surface.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN H. RAO whose telephone number is (571)272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Long Pham/
Primary Examiner, Art Unit 2814

/Steven H Rao/
Examiner, Art Unit 2814